A Novel 5-5.7GHz Low-Power LNA Using Low-Power Techniques

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Abstract. In this paper, a novel 5-5.7GHz low power low noise amplifier (LNA) is designed. It utilizes two stage structures, including common-source structure adopting self-forward-body-bias (SFBB) technique, improved input matching and output matching methods. In 5-5.7GHz band, simulation results shows the design has gain greater than 16.5dB, operating voltage lower than 1V and low noise figure.

Introduction

Growth of wireless communications has resulted in a large number of portable devices. Therefore, the power consumption has also exerted a vital impact on a receiver system due to the battery characteristic and widely use of portable devices. Hence, low power LNA has received more and more interest. Recently, many papers about the low power technology have been presented[1-11]. These techniques are mainly about, current-reuse technique[2,3], SFBB technique[4,5], gm-boosting technique, and so on. In this paper, a novel 5.0-5.7GHz low-power (LP) LNA is proposed. By using two stage amplifier structure and self-forward-body-biasing technique, noise performance can be improved, high gain is achieved and power consumption is saved correspondently. Compared with the LNAs published previously, the presented circuit has superior performance such as flat gain greater than 16.5dB and NF lower than 2.5dB. More importantly, it has 1V operating voltage and only 2.3mW power consumption.

Circuit Implementation

The proposed LNA circuit diagram is presented in Fig.1. The folded cascode structure is used as the input stage.

![Circuit Diagram](image)

Figure 1. The presented low power LNA.

First Stage

Fig.2 indicates the first stage of the presented low power LNA. Suppose that the relation between the input impedance $Z_{in}(s)$, $R_s$ and $\omega_0$ can be expressed as:

$$Z_{in}(s) = \frac{1}{S(C_{o1}+C_{o2})} + S\beta + \omega_0 L_1$$  \hspace{1cm} (1)
where $C_{gs1}$ is the gate-source capacitor used for direct current signal choking. Capacitors and inductors are used to achieve power and noise matching[3]. $Z_{in}(s)$ which is around 50ohm can be got by analyzing and calculating equation (1), the inductor L1 of 5.1nH is got by considering the central frequency is 5.35GHz.

$\text{Figure 2. The proposed LNA input circuit.}$

The Amplification Structure Using Forward-body-bias Technique

To overcome the high voltage problem, SFBB technique is added to lower MOSFET threshold voltage $V_{th}$[2] so as to get low power consumption. $V_{in} = V_{no} + \gamma(\sqrt{\beta V_{th} - V_{in}} - \sqrt{\beta})$, where $V_{in}$ is the voltage between body and source. Therefore, by alternating $V_{in}$, $V_{n}$ is varied, so lower $V_{n}$ is got. And lower supply voltage and finally lower power consumption is realized. M1, M2, R2, R4 form a SFBB structure to achieve the goal mentioned above.

$\text{Figure 3. Small signal model of the CS structure using SFBB technique.}$

The small signal mode of the common source(CS) structure using SFBB technique is shown in Fig.3. The gain of two CS amplifier can be got: $\frac{g_{m1}z_{ik}}{g_{m2}C_{dsk} + j\omega C_{dsn} C_{sik} z_{ik} + 1}$, where $z_{ik}$ is two CS amplifiers load impedance . (K=1,2).

Because LNA gain can be expressed as: $A_{tot} = A_{11}A_{12} \ldots A_{mm}$. Where $A_{mm}$ is the gain of the m stage. (m=1,2,3...).

By combining the factors mentioned above, total gain of the LNA is:

$$A_{tot} = \frac{g_{m1}}{g_{m2}C_{dsk} + j\omega C_{dsn} C_{sik} z_{ik} + 1} \cdot \frac{g_{m2}}{g_{m3}C_{dsk} + j\omega C_{dsn} C_{sik} z_{ik} + 1} \cdot \frac{g_{m3}}{g_{m4}C_{dsk} + j\omega C_{dsn} C_{sik} z_{ik} + 1}$$

(2)

M1, M2 is biased according to [6]. M1,M2,R2,R4 form a SFBB structure to achieve the goal of saving power consumption and noise-canceling. In this circuit, the width to length ratio of transistor M1 is 320 $\mu$m/0.18$\mu$m, the width to length ratio of transistor M2 is 340 $\mu$m/0.18$\mu$m.

Noise Figure

According to[7] and [8], the noise resistance $R_n$, the minimum noise factor $F_{min}$ can be given in the following equation:

$$F_{min} = 1 + 2.4 \frac{\gamma_1}{\alpha_t} \left( \frac{\omega}{\alpha_t} \right)$$

(3)
The transistor M1 gate width can be optimized:

\[
W_{\text{opt}} = \frac{3}{2} \frac{1}{\omega_0 L^* d_{\text{ox}} R_{\text{in}} Q_{\text{sp}}}
\]

where related parameters can be seen in [1].

Because total LNA NF is:

\[
F_{\text{tot}} = F_1 + \frac{F_2 - 1}{A_{v1}} + \cdots + \frac{F_m - 1}{A_{v1} \cdots A_{v(m-1)}}
\]

where \(F_m\) is the m stage noise figure and \(A_{V(m-1)}\) is the gain of the m-1 stage.(m=2,3,4…).

By combining the factors mentioned above, the circuit total noise figure is:

\[
F_{\text{tot}} \approx 1 + 2.4 \frac{\gamma_1}{\alpha_1} \left( \frac{\omega}{\omega_T} \right) + \left[ 2.4 \frac{\gamma_2}{\alpha_2} \left( \frac{\omega}{\omega_T} \right) \right] \left\{ \frac{g_{m1} Z_{x1}}{g_{mb1} C_{db1} + j \omega C_{db1} C_{gb1}} + \frac{Z_{x1}}{C_{db1} + C_{gb1}} \right\}
\]

**Simulation Results**

Simulation performances in Fig.4(a) shows in 5-5.7GHz band the circuit S21 is greater than 16.5dB. Result in Fig.4(b) indicates the NF performance is better than 2.3 dB in 5-5.7GHz band. Fig.4(c) shows S11 is less than -10.2dB. And S22 is lower than -10.5 dB and S12 is lower than -25.1dB. The power consumption is 2.7mW. The size of the circuit is 0.77mm×1.09mm. Performance comparisons are summarized in Table.1.
Table 1. Performance comparisons.

<table>
<thead>
<tr>
<th>Parameters</th>
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Conclusion

The proposed low noise amplifier shows superior performance such as S21 better than 16dB and NF lower than 2.5dB. More importantly, it has lower operating voltage and power consumption. The SFBB is proven to be a promising method to realize the low voltage and low power LNA.

References


