A Highly-cost-effective Area-array Probe-unit as a Key Hardware Technology in Quality Management System for IoT Products

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Abstract. This paper describes the highly-cost-effective high-density area-array probe-unit which consists of four functions, “Densification,” “Fan-out (non-discontinuous),” “Connection,” and “Transformation,” designed and manufactured by our unique monolithic fabrication method, as a key hardware technology of quality management system in a production site for the Internet of Things (IoT), Artificial Intelligence (AI), and Big Data fields. This new probe-unit provides a multiple test/monitor function with high accessibility to I/O density and a high signal integrity structure for providing test signals or collecting massive data between the semiconductors/devices and testers. And this probe-unit is widely available as a versatile interconnection system connecting directly the wafer-level fine-pitch terminals with the test/monitor terminals which is compatible with motherboard technology pitch requirements. At the same time, we have also developed the monolithic fabrication method that an entire matrix probe array with subsequent fan-out patterns and monitor terminal array was created from a single conductive film and formed only by folding like “Origami” (paper-folding). In this innovative method, massive probes and fan-out patterns were designed and manufactured significantly cheaper and faster. We have developed a 22.5-um pitch and 38000-pins-class area-array probe-unit with non-discontinuous fan-out structure without interposer substrates using the monolithic fabrication method and demonstrated the high precision probe array and high productivity.

Introduction
The IoT, AI and Big Data have been important key-words in technology industry in recent years. Growing number of physical objects are being connected to the Internet by realizing the vision of the IoT [1]. Semiconductors and devices inevitably need interrelated requirements of cost effectiveness, thinner and/or smaller form factor, high performance and integration, adding the condition of a significant increase in input/output (I/O) density.

Semiconductors are globally used in the IoT, AI and Big Data fields. The IC trend has always been shrinking die sizes with increasing I/O density, although with the demand for higher performance, so the I/O configuration must be finer-pitch and area-array (or matrix-shape) geometrically, both at the die and the advanced package level. A transition from traditional packages to fan-out wafer-level packages (FOWLP) is inevitably required to achieve maximum connection density and thinner area-array package dimensions, improved electrical and thermal performance especially in mobile markets [2].

As another example of I/O density, a large size display needs also massive area-array fine-pitch I/O points with several tens of thousands of pads for connecting each pixel, which works also test points for on/off display test.

The vision of IoT is to realize the interconnectivity between sensors, actuators, computers and processes. In the process of realization of each IoT, AI and Big Data products, multiple testing or massive data monitoring between the semiconductors/devices and testers are needed. Thus, we must discuss a testability of integrated devices in process. Especially for higher integration device, testing in an early stage is highly important because one defect in one integrated device can ruin the whole
device. Detecting defects can save the unnecessary costs for the subsequent manufacturing steps [3]. Therefore, a factory needs a flexible versatile interconnection system which can connect directly the wafer-level fine-pitch terminals with the test/monitor terminals compatible with motherboard technology pitch requirements in three-dimensional space freely, adding the condition that such related connection devices must be designed and manufactured cheaper and faster.

A representative connection device for silicon process technology pitch requirements is a probe card for detecting semiconductor defect in wafer-level. However, traditional and current probe card technologies are reaching their limits in terms of the performance, pin-shrinking and scalability required to meet the needs of emerging applications. Especially, the massive-pin-count fine-pitch area-array probing has long been one of the biggest challenges in the probe card field. The probing system must be easy to adjust the I/O configuration and easy to connect the test terminals, for coping with various IC technology option flexibly. A current Vertical-MEMS-type used as an area-array probe card has general features below, which are the cost factor from the perspective of cost efficiency and performance [4][5].

1) Probe pins have been traditionally independent parts and handled with highly-skilled assembling process, and per-pin maintenance becomes harder work, as a matrix density increase.
2) High-layer and high-density space-transformers or interposers are used for fan-out patterning.
3) High-layer substrates create many discontinuity points unfavorable to high frequency performance.

We have been researching and accumulating the fine-pitch multi-I/O connection technology, starting with the probe card technology for solving problems above, characterized by the sheet-like-structure probe and fan-out patterning technology [6] [7]. At this time, further developed new structure and manufacturing method were achieved with the following objectives and concepts:

1) Simple structure and manufacture method for high-productivity and cost-effectiveness,
2) Flexible installation or arrangement on a test board/system,
3) as well as Matching the future market requirements.

Application Concept

As the application concept, this probe-unit was designed with the intent to act as a key hardware device in the total quality management system in the production site for IoT, AI, Big Data Products, for achieving the versatile and cost-effective interconnection system connecting directly semiconductor-level fine-pitch terminals with the test/monitor terminals compatible with motherboard technology pitch requirements with easy handling.

The application is expected to be wide-ranging. Figure 1 shows some recommended application of the probe-unit. In Figure 1, type-a is a basic application often used as a probe card for wafer/package test. Type-b shows a parallel test structure for testing multiple chips simultaneously on a wafer for the test cost reduction. In type-c, two terminal-arrays connect each other for connecting the corresponding
two devices electrically. Furthermore, in type-d, an active circuit can be inserted between the two terminal-arrays for adding an active function like signal switching.

**Probe-unit Configuration**

The highly-cost-effective high-density area array probe-unit consists of following four functions, as shown in Figure 2.

![Figure 2. Probe-unit configuration.](image)

**Densification.** This function enables high accessibility to I/O density with wafer-level fine-pitch like IC or IC-package terminals. This part consists of probe-pin array which is accurately compatible with the relative coordinate of target device terminal array. Every probe-pin has spring characteristics independently to the target device terminals and thus can operate to contact with optimal contact forces. Since all the probe-pin of the array were formed by electroforming as an Integrated pattern, even high-pin-count (several tens of thousands of) probe-pins were formed at the same time, while Figure 2 shows the target pad/bump is 22.5 μm-pitch-array as an example.

**Fan-out.** Fan-out means to expand the pitch between pins from the wafer-level fine-pitch in the densification area to the wider motherboard technology pitch. Fan-out patterns were seamlessly formed continuously from each probe to optional test area without any high cost space-transformers/interposers generally used in current probe cards. This characteristic non-discontinuous fan-out pattern structure reduces reflection loss, furthermore, constructing impedance-matching structures easily formed along the signal lines enables high electrical performance.

**Connection.** A fan-out matrix terminal-array was formed for contacting the test/monitor terminal. This part also consists of probe-pin array which is directly connected with each probe-pin in the densification area and has also spring characteristics to easily contact with outer probes or another probe-unit.

**Transformation.** This function is a relative position conversion between the densification probe-array and fan-out matrix terminal-array, and thus enables flexible placement on a board or test system. The length or shape of the fan-out patterns part can be flexibly designed to match the test/monitor equipment.

**Monolithic Fabrication Method**

An entire probe-unit with every four functions above was created from a single conductive film in the following steps. Figure 3 and Figure 4 show the basic concept of the monolithic fabrication method.
**Design-step:** Entire patterns including probe shapes, fan-out patterns, terminal-probe shapes, and insulating film shapes were designed on a single X-Y coordinate plane, and thus every coordinate data were managed as an interrelated in a common coordinate, as shown in Figure 3.

**1st-step:** As a 1st-fabrication stage, all patterns were formed by electroforming of Nickel aminosulfonate two-dimensionally based on the common coordinate designed.

**2nd-step:** As a 2nd-fabrication stage, the final assembly shape was formed only by folding like “Origami” (paper-folding) three-dimensionally from the two-dimensional pattern film of 1st-step, without precision assembly process, as shown in Figure 4.

![Figure 3. Two-dimensional 1st-fabrication stage.](image1)

![Figure 4. Three-dimensional 2nd-fabrication stage.](image2)

**Manufacture and Evaluation**

We have produced and evaluated a probe unit including the specification below:

1) Target bump array of 22.5 μm-pitch staggered area-array with total pins of 38000,
2) Fan-out wiring structure, non-discontinuously expanding from 22.5 μm-bump pitch area to 0.5mm-pitch-matrix terminal, and
3) Two probes array per a bump (Kelvin-type) included.

The following results were obtained:

1) Probe-array accuracy: +/-4 μm at X-directional, +/-8 μm at Y-directional
2) Coplanarity of probe-tips: below 10 μm
3) Durability test: within the above spec at a million touchdowns
4) Contact resistance variation at continuous test up to 1000 touchdowns: within 0.2 ohm

**Conclusion**

We achieved the high-density area-array probe-unit and the innovative monolithic fabrication method, which provide the following solution for the total quality management system in the production site for IoT, AI, Big Data Products.

**High-density area-array I/O contacting:** for the devices which inevitably need interrelated requirements of thinner and/or smaller size, high performance and integration, with the condition of a significant increase in I/O density.

**Highly-cost-effective simple design and fabrication:** by the method that the entire matrix probe array with subsequent fan-out patterns and monitor terminal array was created from a single
conductive film and formed only by folding, which enables even higher pin-count probe-unit to be
designed and manufactured significantly cheaper and faster.

**Flexible installation or arrangement on a test board/system:** by easily contacting the
customized fan-out matrix terminal-array with outer probes or another probe-unit.

We have developed a 22.5-um pitch and 38000-pins-class area-array probe-unit with
non-discontinuous fan-out structure without interposer substrates and demonstrated the high
precision probe array and high productivity.

**References**


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