Design of a Frequency Doubler Circuit for Suppressing odd Harmonics

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ABSTRACT

In this paper, a doubler circuit which can suppress odd harmonics is designed by using the non-linear characteristics of field effect transistor (FET) and bipolar junction transistor (BJT) devices. The frequency doubler consists of three parts: small signal full wave rectifier circuit, frequency doubler circuit and band-pass filter circuit. It realizes fundamental and third harmonics suppression by rectifying the input signal of single FET frequency doubler. Meanwhile, the output power is twice as high as that of single FET frequency doubler (3dB higher). Circuit simulation results indicate that when the input fundamental voltage amplitude is 0.5V, the output voltage amplitude of second harmonics is 0.342V, the fundamental suppression is greater than 48.85dBc, and the third harmonic suppression is greater than 34.39dBc. Compared with the traditional single FET frequency doubler, this design improves the frequency conversion efficiency.

KEYWORDS
Frequency Doubler, Harmonics Suppression, Rectifier.

INTRODUCTION

Frequency doubler is a kind of circuit commonly used in radar and communication system. It is a key module of frequency multiplier link and frequency synthesizer. In theory, all non-linear electronic devices can be adopted to realize frequency multiplication, but in practice, diodes and active three-terminal devices are more commonly used. Frequency doubler circuit can effectively extract the required harmonics while suppressing the fundamental and unnecessary harmonics. The common single transistor frequency doubler circuit has the advantages of simple structure and easy realization. However, with low output power, only part of the input signal power is utilized, and its ability to suppress useless harmonics is poor. Therefore, this paper designs a frequency doubler circuit which can suppress odd harmonics by using FET and BJT. The circuit keeps the positive half-cycle part of the input small signal unchanged by the transistor, and reverses the negative half-cycle part phase for 180°. Then the signal is input into the depletion-type FET gate. The high-order harmonics are generated by the non-linearity of the FET gate’s DC bias in the pinch-off state of $V_{gs}=V_{gs}(off)$. Then, the dipole harmonic phases of the drain signal

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output terminal of the FET are the same and the power is increased after superposition; the odd harmonic phases are opposite and the power decreases[1-2], thus forming a high efficiency frequency doubler.

**CIRCUIT DESIGN**

Compared with diodes, the outstanding advantage of using FET and BJT to design frequency multiplier is that it can obtain frequency multiplier gain and provide effective isolation between input and output. In the active frequency multiplier composed of field effect transistors, the most important index is transconductance $g_m$, which can be equivalent to a non-linear voltage-controlled current source. For single-transistor FET pinch-off frequency multiplier, it is very important to provide a reasonable bias voltage, which is closely related to output power, efficiency and stability. In a single-transistor pinch-off FET frequency multiplier, the gate DC bias voltage $V_{gs}$ is always biased near the pinch-off voltage $V_{gs}(off)$. Drain current $I_{ds}$ is a spike pulse current and contains abundant harmonics due to the pinch-off effect of the FET[3]. At this time, the drain current waveform can be treated as half of a cosine pulse sequence, as is shown in Formula (1):

$$I_{ds}(t) = I_0 + I_1 \cos \omega t + I_2 \cos 2\omega t + ...$$

$$I_0 = I_{max} \frac{2\tau}{\pi T}$$

$$I_n = I_{max} \frac{4\tau}{\pi T} \left| \frac{\cos(n\pi\tau/T)}{1-(2n\pi\tau/T)^2} \right|, n \geq 1$$

In the formula: $I_{max}$ is the peak value of drain current, while $\tau$ is the turn-on time in each cycle. Formula (1) shows that $I_n$ decreases as the value of $n$ increases, so this frequency multiplier cannot be used for high-order frequency multiplication, but can completely satisfy frequency doubling. However, the components whose amplitudes are less than $V_{gs}(off)$ in the gate input signal are not effectively utilized. It can be seen that if the signal is fully rectified at the gate input of the field effect transistor multiplier, the drain current $I_{ds}$ becomes a continuous pulse with a pulse frequency of $2f_0$. In this way, the second harmonic components of the output current $I_{ds}$ can be greatly increased and the odd harmonic can be suppressed.

The circuit structure of the active frequency doubler designed in this paper is shown in Figure 1. According to its function, the circuit can be divided into three main parts: small signal rectifier circuit, frequency doubler circuit and band-pass filter circuit.
Figure 1. Circuit diagram of the active frequency doubler.

The main function of small signal rectifier circuit is to make the negative half period part of input signal produce a phase shift of 180°, and the signal DC bias is placed on the negative voltage of -Vbe(on)(Vbe(on): the turn-on voltage of base-emitter junction). When the sinusoidal signal is input and the positive half period of the signal Vi > 0V, the emitter junction of NPN triode Q1 is positively biased, the base-emitter voltage is greater than the turn-on voltage Vbe(on), and triode Q1 is turned on. At this time, the base-emitter voltage of PNP triode Q3 is smaller than the turn-on voltage Vbe(on) and triode Q3 is cut off. Therefore, the current flows from R1 to R3 through triode Q1 and then through power source -Vbe(on) to the ground. The current on R3 is bottom-up, and the voltage on its lower side is -Vbe(on) +R3*Ice1, which forms the positive half period of the input signal of M1 FET. Similarly, when the negative half-cycle of the signal Vi < 0V, triode Q1 is cut off, the emitter-base voltage of triode Q3 is greater than the turn-on voltage Vbe(on), and PNP triode Q3 is turned on. Then, NPN triode Q2 is turned on, the current flows from R2 through triode Q3 to resistance R5, then through triode Q2, R3, and the power source -Vbe-(on) to the ground. The current on R3 is still bottom-up, and the voltage on its lower side is -Vbe(on)+R3*Ice2, thus forming another half period of the input signal of M1 FET[4]. In order to ensure that Ice1≈Ice2 when the absolute value of positive and negative half-cycle voltages are the same, R2=k*β^2*R1 is generally selected, where β is the current amplification factor of the NPN triode.

Figure 2. Transition characteristic curves of drain-source current Ids and gate-source voltage Vgs when Vds is equal to 2V.
When the drain-source voltage $V_{ds}$ of the depletion-type FET is constant, the transition characteristic curves of drain-source current $I_{ds}$ and gate-source voltage $V_{gs}$ are shown in Figure 2, where $V_{gs(\text{off})}$ represents the value of $V_{gs}$ when the gate-source clamp occurs.

If $V_{gs(\text{off})}$ of depletion-type FET $M1$ is approximately equal to $V_{be(\text{on})}$, the field effect transistor works in the region with the largest curvature of the transfer characteristic curve. At this time, the output current $I_{ds}$ of $M1$ contains abundant high-order harmonics, and because the frequency of the gate input signal shown in Figure 3 is $2f_0$, the $2f_0$ component of the output signal has the maximum power, and the fundamental and odd harmonic signals can be suppressed effectively. In this way, purer second harmonic signals can be obtained[5]. Meanwhile, since the field effect transistor works in the constant current region, this circuit structure also has higher frequency conversion gain and efficiency.

**SIMULATION RESULTS**

In order to verify the performance of the frequency doubler, the circuit of Figure 1 is simulated by Advanced Design System 2016, where $R1 = 10\Omega$, $R2 = 80000\Omega$, $R3 = 30\Omega$, $R4 = 20\Omega$, $R5 = 150\Omega$, $R6 = 100\Omega$, $R7 = 50\Omega$, $\beta$ of triode $Q1$, $Q2 = 200$, $\beta$ of triode $Q3 = 30$, $V_{be(\text{on})} = 0.75V$, $V_d = 2V$, $V_c = 3V$. The input signal $f_0 = 1\text{MHz}$ and $V_i = 0.5V$ are selected, and the Bessel bandpass filter is used at the output to simulate the frequency doubler circuit. The output voltage waveform of the full-wave rectifier circuit is shown in Figure 3.

![Output voltage waveform of the full-wave rectifier circuit.](image)

From the output waveform of the rectifier circuit, it can be seen that the negative half-cycle part of the input signal has undergone a phase reversal of $180^\circ$, and the DC bias is near $-V_{be(\text{on})}$, the amplitude of the signal after rectification is close to $0.3V$, but the positive and negative period waveforms are not identical.

Due to the fact that the smaller the order of harmonics output by FET itself, the higher the harmonic power, the suppression of fundamental and third harmonics is still poor despite the addition of a circuit that can realize this function. Therefore, it is necessary to add a bandpass filter after the output of the doubled frequency part.
Bessel filter with center frequency of 2MHz, Passband Edge-to-Edge Width of 0.5MHz and stopband attenuation of 3dB is selected. After adding Bessel type bandpass filter, the harmonic simulation results and spectrum diagrams of the frequency doubler are shown in Figure 4 and Figure 5 respectively. The simulation results show that the fundamental suppression is 48.85 dBC, the third harmonic suppression is 34.39 dBC, the fourth harmonic suppression is 54.62 dBC, and the fifth harmonic suppression is greater than 62.82 dBC.

CONCLUSION

Starting from the principle of active frequency multiplier, this paper focuses on the analysis and theoretical derivation of the working principle of each unit circuit, designs a frequency doubler circuit with excellent output power and harmonic suppression performance, and simulates and verifies the circuit with software ADS 2016. The simulation results show that when the input fundamental voltage amplitude is 0.5V, the output voltage amplitude of the second harmonic is 0.342V, the fundamental suppression is greater than 48 dB, and the third harmonic suppression is greater than 34 dB. This frequency doubler maintains low power consumption while achieving high output power and high odd harmonic
suppression. The circuit structure of frequency doubler presented in this paper provides a reference for the design of signal source in high-speed communication system, and provides a way of thinking for the design of low-loss, broadband frequency doubler circuit in the future. We will mainly study the phase noise characteristics of the frequency multiplier and analyze the conversion loss of the frequency multiplier more deeply.

ACKNOWLEDGMENT

This work was supported by the National Key Research and Development Program of China, grant number 2016YFC0800400, and by National Natural Science Foundation of China, grant number 61731001.

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